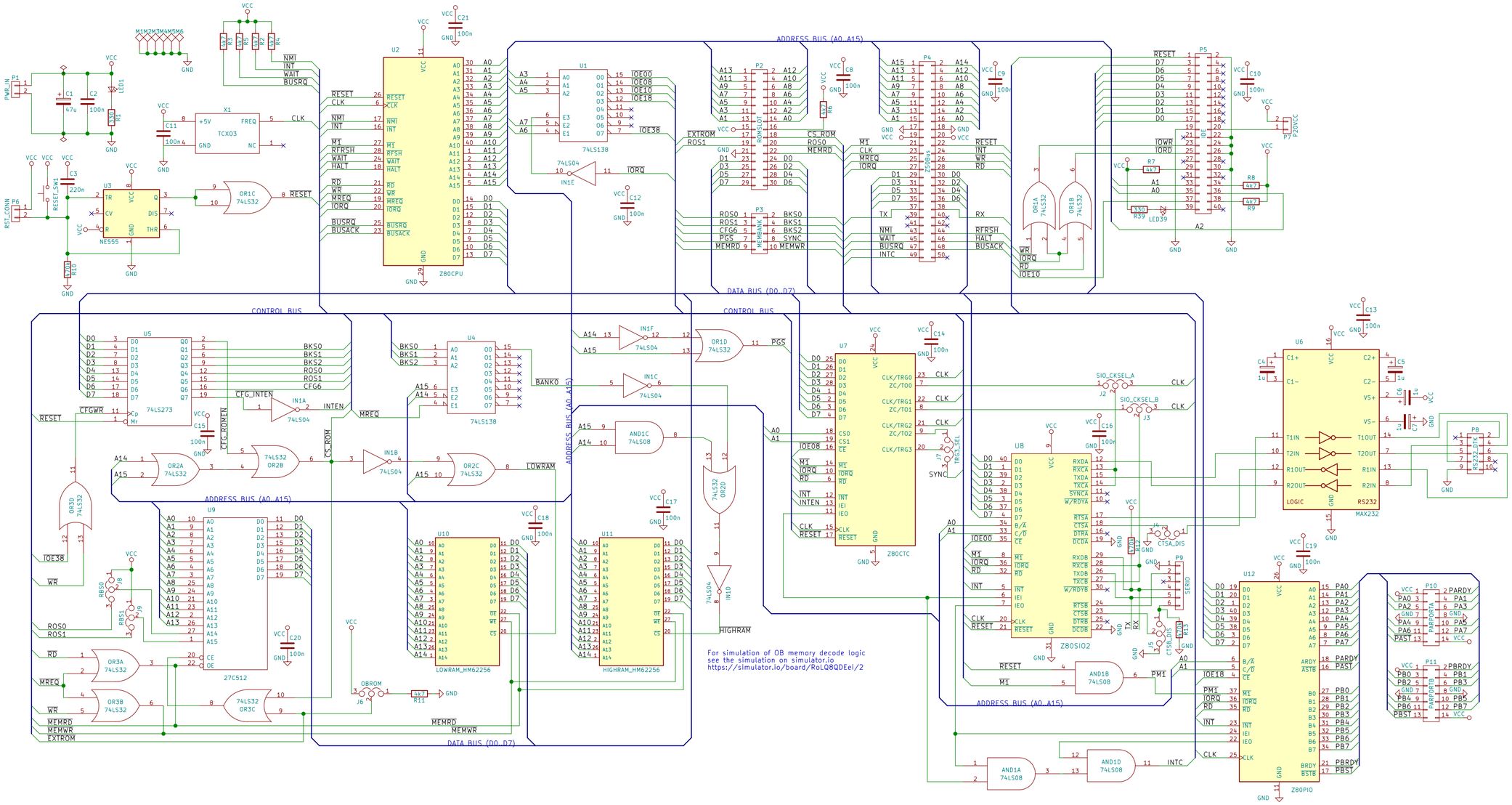
ADDRESS BUS (A0..A15)
DATA BUS (D0..D7)
CONTROL BUS
Z80CPU
74LS138
ROMSLOT
MEMBANK
Z80CTC
Z80SIO2
Z80PIO
MAX232
NE555
TCXO3
27C512
LOWRAM_HM62256
HIGHRAM_HM62256
For simulation of OB memory decode logic
see the simulation on simulator.io
https://simulator.io/board/RoLQ8QDEei/2
Design by Jon Langseth
Zilog Z80 based system w/banked memory
Expandable Single Board Computer
LINC
Sheet: /
File: L80S1D.sch
Title: LINC80 Computer version 1
Size: A2
Date: 2018-03-13
Rev: 4.9
KiCad E.D.A. kicad 4.0.7
Id: 1/1