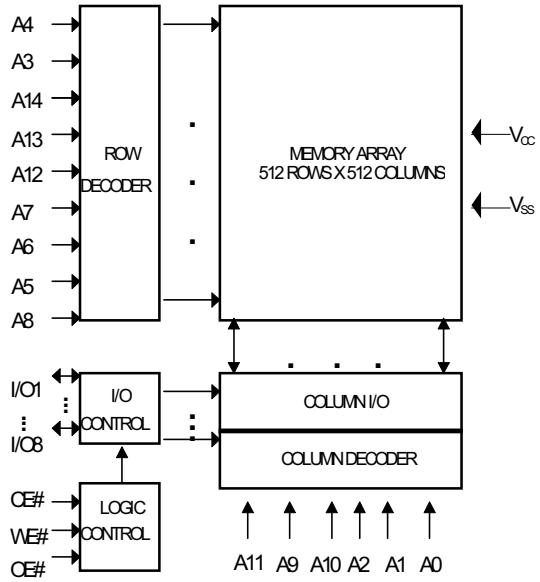
## FEATURES

- Fast access time : 8/10/12/15 ns (max.)
- Low operating power consumption : 80 mA (typical)
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Package : 28-pin 300 mil skinny PDIP
  28-pin 300 mil SOJ
  28-pin 330 mil SOP
  28-pin 8x13.4mm TSOP-I

## FUNCTIONAL BLOCK DIAGRAM




## PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| A0 - A14 | Address Inputs |
| I/O1 - I/O8 | Data Inputs/Outputs |
| CE# | Chip Enable Inputs |
| WE# | Write Enable Inputs |
| OE# | Output Enable Inputs |
| $V_{CC}$ | Power Supply |
| $V_{SS}$ | Ground |

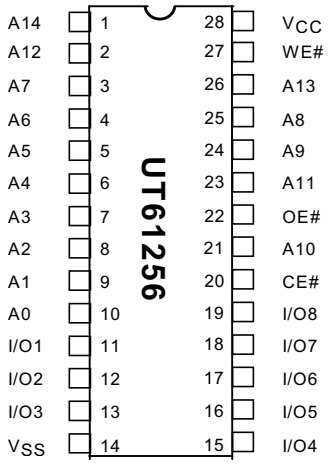
## GENERAL DESCRIPTION

The UT61256 is a 262,144-bit high-speed CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

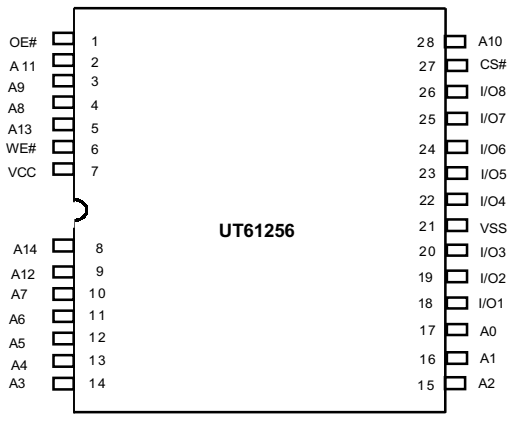
The UT61256 is designed for high-speed system applications. It is particularly suited for use in high-density high-speed system applications.

The UT61256 operates from a single 5V power supply and all inputs and outputs are fully TTL compatible.

## PIN CONFIGURATION




**PDIP/SOP/SOJ**




**TSOP-I**

## ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Terminal Voltage with Respect to Vss | $V_{TERM}$ | -0.5 to +6.5 | V |
| Operating Temperature | $T_A$ | 0 to +70 | ℃ |
| Storage Temperature | $T_{STG}$ | -65 to +150 | ℃ |
| Power Dissipation | $P_D$ | 1 | W |
| DC Output Current | $I_{OUT}$ | 50 | mA |
| Soldering Temperature (under 10 sec) | Tsolder | 260 | ℃ |

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

## TRUTH TABLE

| MODE | CE# | OE# | WE# | I/O OPERATION | SUPPLY CURRENT |
|---|---|---|---|---|---|
| Standby | H | X | X | High - Z | $I_{SB}$,$I_{SB1}$ |
| Output Disable | L | H | H | High - Z | $I_{CC}$ |
| Read | L | L | H | $D_{OUT}$ | $I_{CC}$ |
| Write | L | X | L | $D_{IN}$ | $I_{CC}$ |

Note: H = $V_{IH}$, L=$V_{IL}$, X = Don't care.

## DC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5V± 10%, $T_A$ = 0℃ to 70℃)

| PARAMETER | SYMBOL | TEST CONDITION | | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | | | 2.2 | $V_{CC}$+0.5 | V |
| Input Low Voltage | $V_{IL}$ | | | - 0.5 | 0.8 | V |
| Input Leakage Current | $I_{LI}$ | $V_{SS} \leqq V_{IN} \leqq V_{CC}$ | | - 1 | 1 | μA |
| Output Leakage Current | $I_{LO}$ | $V_{SS} \leqq V_{I/O} \leqq V_{CC}$<br>CE# = $V_{IH}$ or OE# = $V_{IH}$<br>or WE# = $V_{IL}$ | | - 1 | 1 | μA |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = - 4mA | | 2.4 | - | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8mA | | - | 0.4 | V |
| Operating Power Supply Current | $I_{CC}$ | CE# = $V_{IL}$ , $I_{I/O}$ = 0mA<br>Cycle=Min. | - 8 | - | 190 | mA |
| | | | - 10 | - | 180 | mA |
| | | | - 12 | - | 160 | mA |
| | | | - 15 | - | 140 | mA |
| Standby Power Supply Current | $I_{SB}$ | CE# = $V_{IH}$ | | - | 30 | mA |
| | $I_{SB1}$ | CE#≧$V_{CC}$-0.2V | | - | 5 | mA |

## CAPACITANCE ($T_A$=25℃, f=1.0MHz)

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | - | 8 | pF |
| Input/Output Capacitance | $C_{I/O}$ | - | 10 | pF |

Note : These parameters are guaranteed by device characterization, but not production tested.

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | 0V to 3.0V |
| Input Rise and Fall Times | 3ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | $C_L$=30pF, $I_{OH}/I_{OL}$=-4mA/8mA |

## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5V± 10% , $T_A$ = 0℃ to 70℃)

### (1) READ CYCLE

| PARAMETER | SYMBOL | UT61256-8 | | UT61256-10 | | UT61256-12 | | UT61256-15 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | $t_{RC}$ | 8 | - | 10 | - | 12 | - | 15 | - | ns |
| Address Access Time | $t_{AA}$ | - | 8 | - | 10 | - | 12 | - | 15 | ns |
| Chip Enable Access Time | $t_{ACE}$ | - | 8 | - | 10 | - | 12 | - | 15 | ns |
| Output Enable Access Time | $t_{OE}$ | - | 4 | - | 5 | - | 6 | - | 7 | ns |
| Chip Enable to Output in Low Z | $t_{CLZ*}$ | 2 | - | 2 | - | 3 | - | 4 | - | ns |
| Output Enable to Output in Low Z | $t_{OLZ*}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Chip Disable to Output in High Z | $t_{CHZ*}$ | - | 4 | - | 5 | - | 6 | - | 7 | ns |
| Output Disable to Output in High Z | $t_{OHZ*}$ | - | 4 | - | 5 | - | 6 | - | 7 | ns |
| Output Hold from Address Change | $t_{OH}$ | 3 | - | 3 | - | 3 | - | 3 | - | ns |

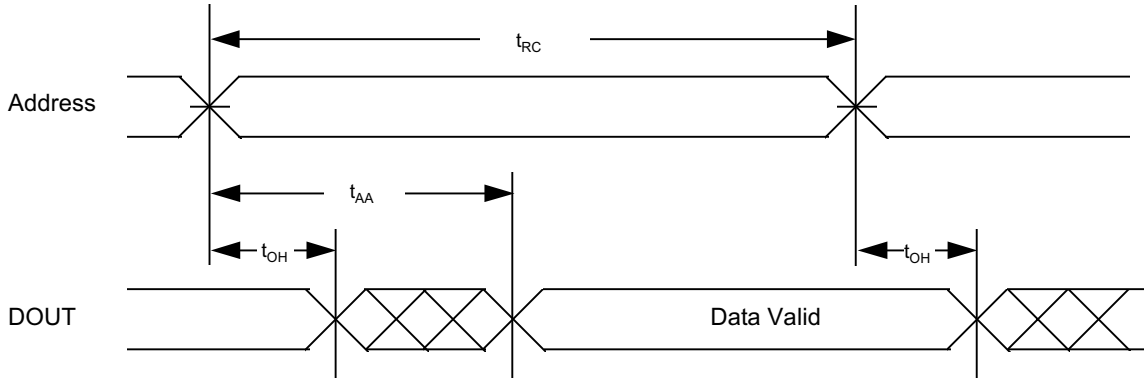
### (2) WRITE CYCLE

| PARAMETER | SYMBOL | UT61256-8 | | UT61256-10 | | UT61256-12 | | UT61256-15 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Write Cycle Time | $t_{WC}$ | 8 | - | 10 | - | 12 | - | 15 | - | ns |
| Address Valid to End of Write | $t_{AW}$ | 6.5 | - | 8 | - | 10 | - | 12 | - | ns |
| Chip Enable to End of Write | $t_{CW}$ | 6.5 | - | 8 | - | 10 | - | 12 | - | ns |
| Address Set-up Time | $t_{AS}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Write Pulse Width | $t_{WP}$ | 6.5 | - | 8 | - | 9 | - | 10 | - | ns |
| Write Recovery Time | $t_{WR}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Data to Write Time Overlap | $t_{DW}$ | 5 | - | 6 | - | 7 | - | 8 | - | ns |
| Data Hold from End of Write Time | $t_{DH}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Output Active from End of Write | $t_{OW*}$ | 1.5 | - | 2 | - | 3 | - | 4 | - | ns |
| Write to Output in High Z | $t_{WHZ*}$ | 5 | | - | 6 | - | 7 | - | 8 | ns |

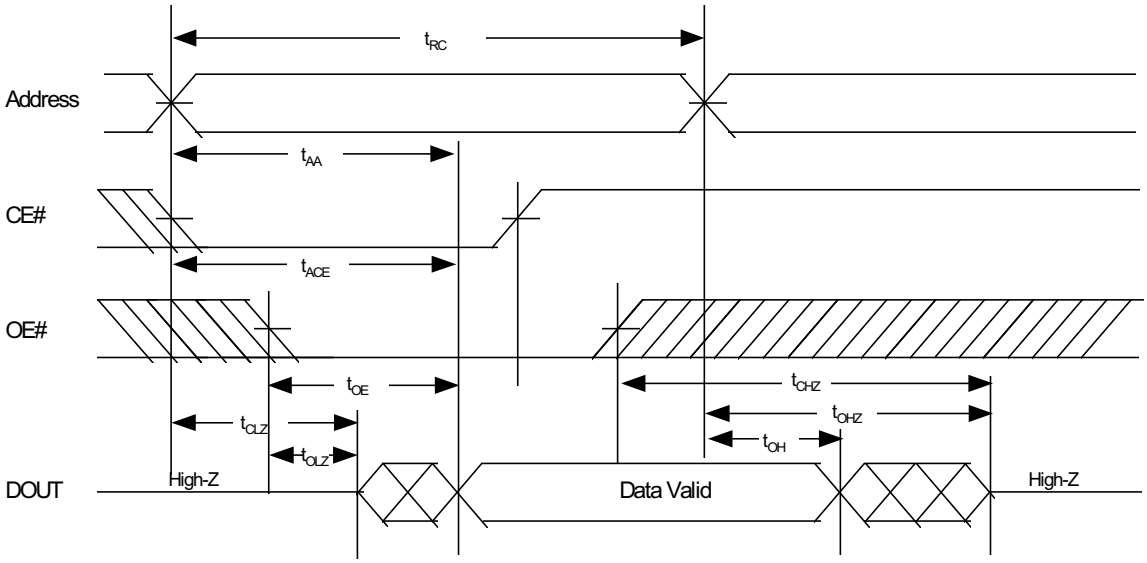
*These parameters are guaranteed by device characterization, but not production tested.

## TIMING WAVEFORMS

**READ CYCLE 1** (Address Controlled) (1,2,4)

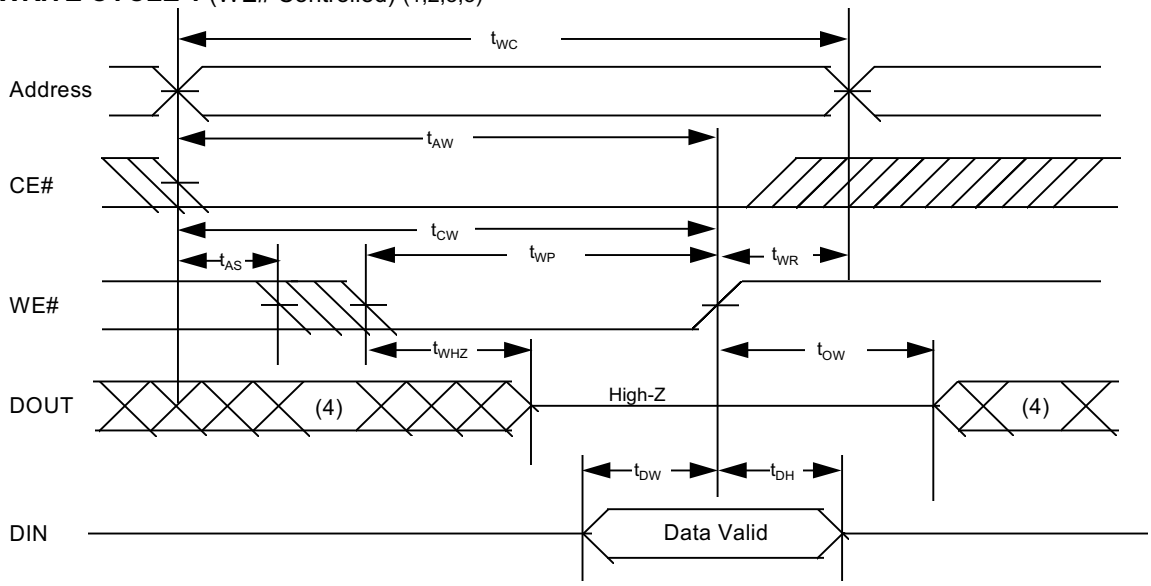



**READ CYCLE 2** (CE# and OE# Controlled) (1,3,5,6)

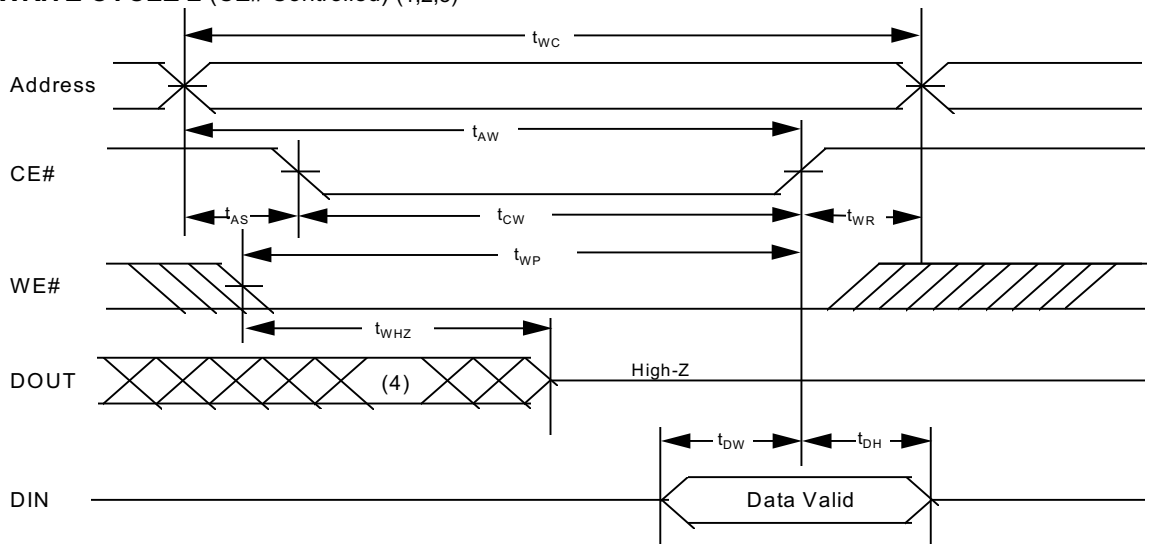



Notes :
1. WE# is HIGH for read cycle.
2. Device is continuously selected CE#=$V_{IL}$.
3. Address must be valid prior to or coincident with CE# transition; otherwise $t_{AA}$ is the limiting parameter.
4. OE# is LOW.
5. $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$ and $t_{OHZ}$ are specified with $C_L$ = 5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, $t_{CHZ}$ is less than $t_{CLZ}$, $t_{OHZ}$ is less than $t_{OLZ}$.

**WRITE CYCLE 1** (WE# Controlled) (1,2,3,5)



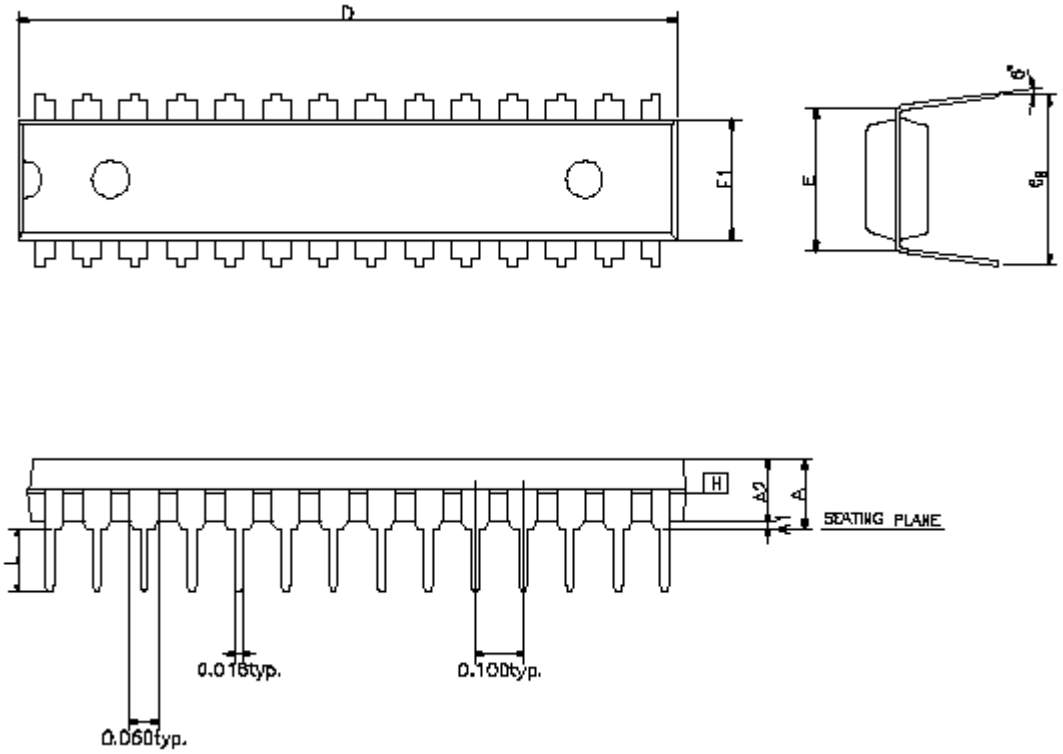

**WRITE CYCLE 2** (CE# Controlled) (1,2,5)




Notes :
1. WE# or CE# must be HIGH during all address transitions.
2. A write occurs during the overlap of a low CE# and a low WE#.
3. During a WE# controlled with write cycle with OE# LOW, $t_{WP}$ must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
5. If the CE# LOW transition occurs simultaneously with or after WE# LOW transition, the outputs remain in a high impedance state.
6. $t_{OW}$ and $t_{WHZ}$ are specified with $C_L$ = 5pF. Transition is measured ± 500mV from steady state.

## PACKAGE OUTLINE DIMENSION

28 pin 300 mil skinny PDIP PACKAGE OUTLINE DIMENSION

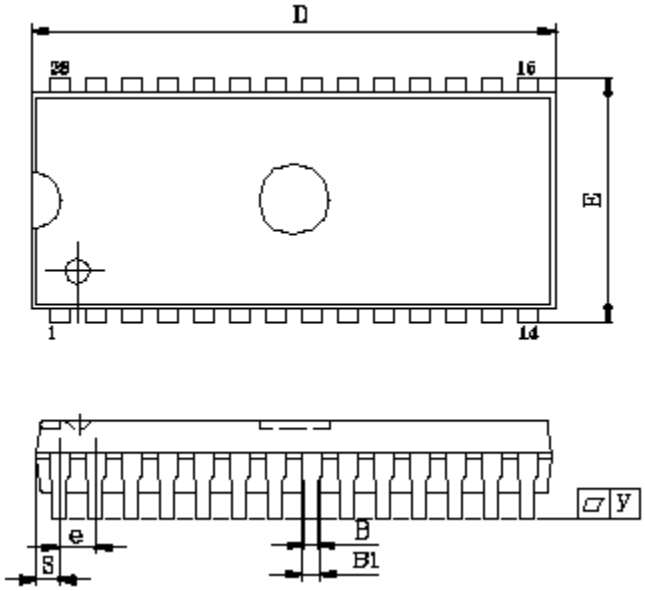


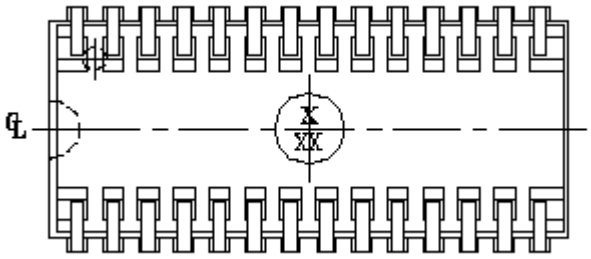

| UNIT / SYMBOL | MIN | NOR. | MAX |
|---|---|---|---|
| A | - | - | 0.210 |
| A1 | 0.015 | - | - |
| A2 | 0.125 | 0.130 | 0.135 |
| D | 1.385 | 1.390 | 1.400 |
| E | | 0.310 BSC | |
| E1 | 0.283 | 0.288 | 0.293 |
| L | 0.115 | 0.130 | 0.150 |
| eB | 0.330 | 0.350 | 0.370 |
| $\Theta^\circ$ | 0 | 7 | 15 |

**Note：**

**1. JEDEC OUTLINE：N / A**

28 pin 300 mil SOJ PACKAGE OUTLINE DIMENSION



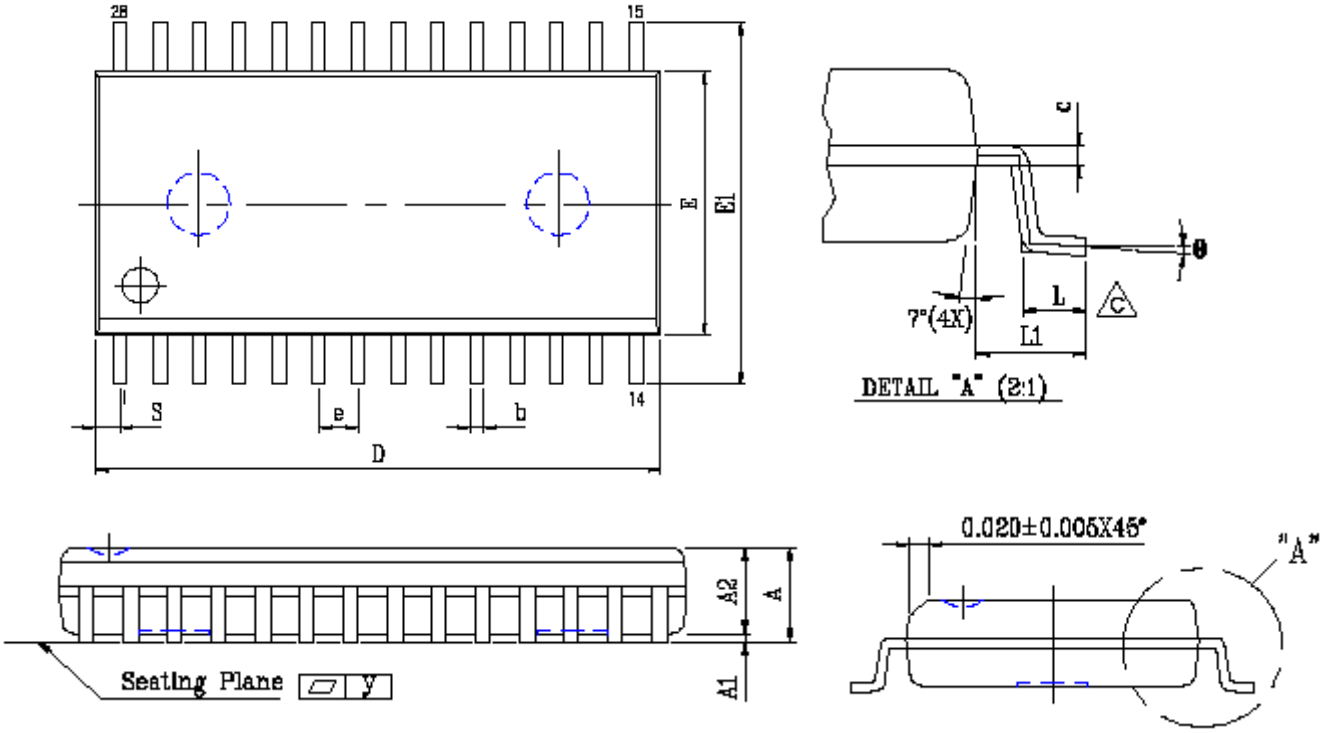

| UNIT / SYMBOL | INCH(BASE) | MM(REF) |
|---|---|---|
| A | 0.148 (MAX) | 3.759 (MAX) |
| A1 | 0.026(MIN) | 0.660(MIN) |
| A2 | 0.100± 0.005 | 2.540± 0.127 |
| B | 0.018 (TYP) | 0.457(TYP) |
| B1 | 0.028 (TYP) | 0.711(TYP) |
| c | 0.010 (TYP) | 0.254 (TYP) |
| D | 0.710 (TYP) | 18.034 (TYP) |
| E | 0.335(TYP) | 8.509(TYP) |
| E1 | 0.3 (TYP) | 7.620(TYP) |
| e | 0.050 (TYP) | 1.270 (TYP) |
| L | 0.087± 0.010 | 2.210± 0.254 |
| S | 0.030 (TYP) | 0.762 (TYP) |
| Y | 0.003(MAX) | 0.076(MAX) |

△D

Note:

1. S/E/D DIM. NOT INCLUDEING MOLD FLASH.
2. THE END FLASH IN PACKAGE LENGTHWISE IS NOT MORE THE 10 MILS EACH SIDE.

**28 pin 330 mil SOP Package Outline Dimension**




| SYMBOL \ UNIT | INCH(BASE) | MM(REF) |
|---|---|---|
| A | 0.120 (MAX) | 3.048 (MAX) |
| A1 | 0.002(MIN) | 0.05(MIN) |
| A2 | 0.098± 0.005 | 2.489± 0.127 |
| b | 0.016 (TYP) | 0.406(TYP) |
| c | 0.010 (TYP) | 0.254(TYP) |
| D | 0.728 (MAX) | 18.491 (MAX) |
| E | 0.350 (MAX) | 8.890 (MAX) |
| E1 (B) | 0.465± 0.012 | 11.811± 0.305 |
| e | 0.050 (TYP) | 1.270(TYP) |
| L (C) | 0.05 (MAX) | 1.270 (MAX) |
| L1 | 0.067± 0.008 | 1.702± 0.203 |
| S | 0.047 (MAX) | 1.194 (MAX) |
| y (E) | 0.003(MAX) | 0.076(MAX) |
| θ | 0°～10° | 0°～10° |

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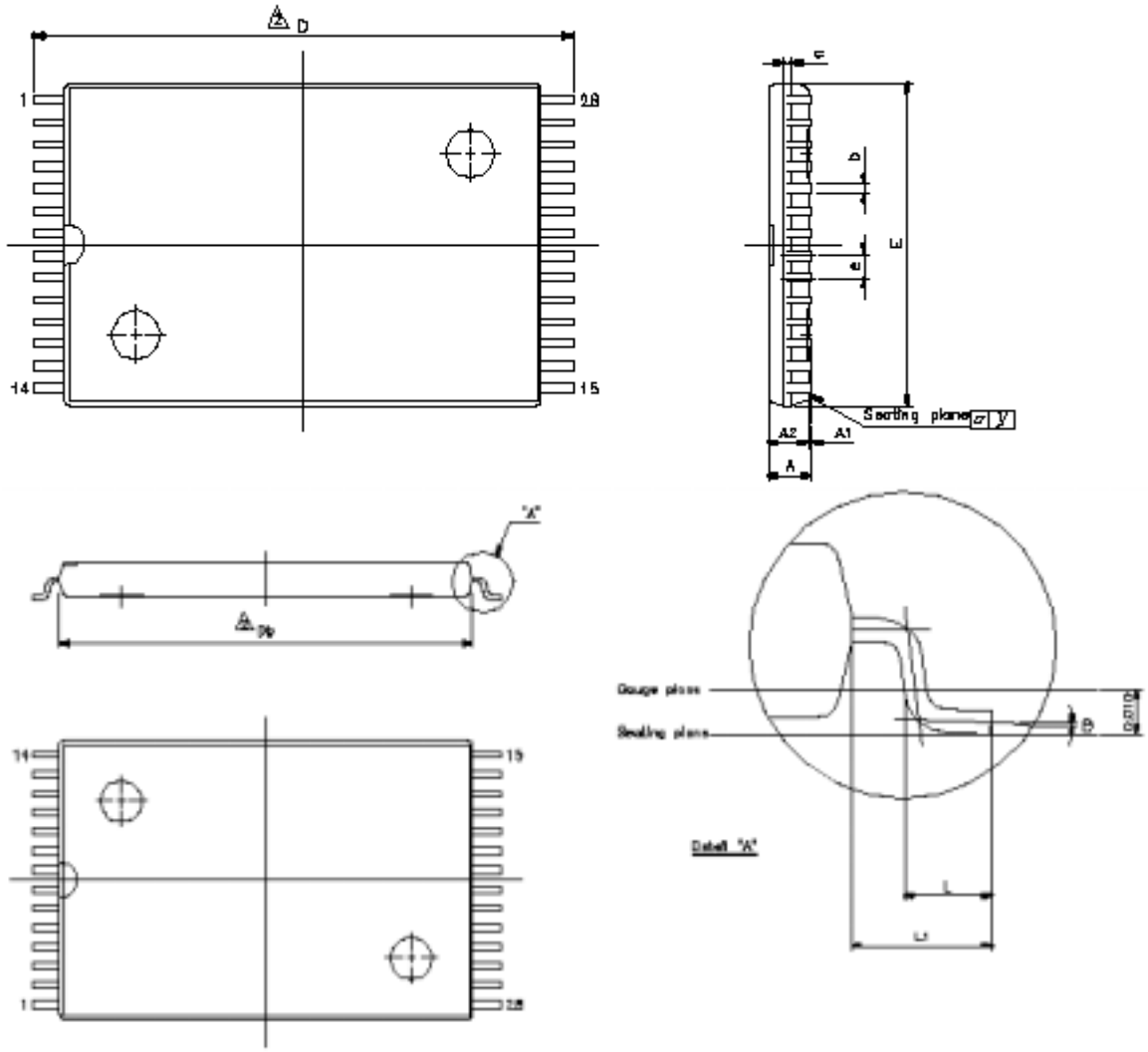
**28 pin 8x13.4mm TSOP-I Package Outline Dimension**




| UNIT / SYMBOL | INCH(BASE) | MM(REF) |
|---|---|---|
| A | 0.047 (MAX) | 1.20 (MAX) |
| A1 | 0.004± 0.002 | 0.10± 0.05 |
| A2 | 0.039± 0.002 | 1.00± 0.05 |
| b | 0.006 (TYP) | 0.15(TYP) |
| c | 0.010 (TYP) | 0.254(TYP) |
| 2 Db | 0.465± 0.004 | 11.80± 0.10 |
| E | 0.315± 0.004 | 8.00± 0.10 |
| e | 0.022 (TYP) | 0.55(TYP) |
| 2 D | 0.528± 0.008 | 13.40± 0.20 |
| 2 L | 0.020± 0.004 | 0.50± 0.10 |
| 2 L1 | 0.0315± 0.004 | 0.80± 0.10 |
| 5 y | 0.08(MAX) | 0.003(MAX) |
| Θ | 0°～5° | 0°～5° |

Note：
E dimension is not including end flash
The total of both sides' end flash is
Not above 0.3mm.

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## ORDERING INFORMATION

| PART NO. | ACCESS TIME (ns) | PACKAGE |
|---|---|---|
| UT61256KC-15 | 15 | 28PIN SKINNY PDIP |
| UT61256SC-15 | 15 | 28PIN SOP |
| UT61256JC-8 | 8 | 28PIN SOJ |
| UT61256JC-12 | 12 | 28PIN SOJ |
| UT61256JC-15 | 15 | 28PIN SOJ |
| UT61256LS-8 | 8 | 28PIN TSOP-I |
| UT61256LS-12 | 12 | 28PIN TSOP-I |
| UT61256LS-15 | 15 | 28PIN TSOP-I |